An Analytical Metal Resistance Model and Its Application for Sub-22-nm Metal-Gate CMOS

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***Abstract*— Gate resistance, middle of line resistance, and back end of line resistance in modern metal-gate CMOS increase drastically as the dimensions of the gates, interconnects and vias scale down close to or below the bulk electron mean free paths (MFPs) of the metal materials. These resistances, especially the gate resistance, impose more and more significant RC delay to CMOS circuits and become significant concerns in sub-22-nm CMOS. In order to optimize the metal-gate materials and structures for low resistance, accurate metal resistance model is needed. In this letter, we propose an analytical metal resistance model applicable for metal wires and films even with sub-MFP sizes. Our model includes scattering effects from surfaces, interfaces, and grain boundaries, and has been successfully verified on *W* metal gates with the feature sizes ranging from 20 to 70 nm.**

***Index Terms*— Metal resistance, gate resistance, analytical model, metal gate, scattering, CMOS.**

I. Introduction

AS THE transistors down-scale, the gate delay becomes more and more prominent due to increasing gate resistivity [1]. Although metal gates are adopted in sub-22 nm CMOS, due to severe surface, interface and grain boundary scattering, a metal gate's resistivity is significantly larger than the metal's bulk resistivity [2]. To come up with strategies for reducing metal gates' resistivity, accurate metal resistance model is needed. Advanced gate-metal stack using the replacement process is composed of multiple layers including the work-function metals (WFMs) and low-resistance electrode [2]. A complete metal resistance model should include not only the phonon, surface and grain boundary scatterings within metal layer, but also the metal layer interface scattering. The existing analytical combined models [3]–[6] have good fit with the measurement for metal wires of large sizes (>MFP) but have deteriorating fit for metal wires of small sizes (≤MFP). In this letter, we report an analytical metal resistance model applicable for metal wires and films even with sub-MFP sizes. Our model was successfully verified on W metal gates with feature sizes ranging from 20 to 70 nm.

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II. Existing Analytical Models

FS Model for Surface Scattering: Surface scattering is usually described by Fuchs-Sondheimer (FS) model [7], [8]. FS model links the resistivity of a metal film after surface scattering (ρ_s) with the metal's bulk resistivity (ρ_0) assuming diffuse and elastic electron scatterings occur at the metal surfaces. A parameter 'p' (between 0 and 1) is used to denote the fraction of electrons that would experience elastic scattering at the surfaces. An analytical model

$$\frac{\rho_s}{\rho_0} = 1 + 0.46 \times (1-p) \times \left(\frac{\lambda_0}{w} + \frac{\lambda_0}{h}\right) \quad (1)$$

for a rectangular metal wire of width-w and height-h matches the numerical solution of FS model within 5% of error [3], [5], [9]. The λ_0 in Eq. (1) is the metal's bulk MFP which originates from the calculation of electrons' scattering rate in the body of the metal wire without the effect from the surfaces [7], [8].

MS Model for Grain Boundary Scattering: Mayadas-Shatzkes (MS) model is widely adopted for modeling the grain boundary scattering [10]. The effect of grain boundary scattering is treated as series of imaginary planes with reflectivity of 'R' placed with average distances of 'D' (the average grain size) perpendicular to the direction of current flow. The resistivity after the effect of grain boundary scattering (ρ_{gr}) is

$$\rho_{gr} = \frac{\rho_0}{1 - \frac{3\alpha}{2} + 3\alpha^2 - 3\alpha^3 \ln(1+\frac{1}{\alpha})} \; (\alpha = \frac{\lambda_0}{D}\frac{R}{1-R}). \quad (2)$$

Combined Models: The existing analytical combined models were built by combining FS model with MS model via Matthiessen's rule [3]–[6]. Since Matthiessen's rule assumes that all scattering mechanisms are independent, the total resistivity (ρ_{total}) of a metal structure can be expressed as the sum of the contributions from phonon scattering (ρ_0), surface scattering ($\rho_s - \rho_0$) and grain boundary scattering ($\rho_{gr} - \rho_0$):

$$\rho_{total} = \rho_0 + (\rho_s - \rho_0) + (\rho_{gr} - \rho_0) = \rho_s + \rho_{gr} - \rho_0. \quad (3)$$

Using Eq. (1) for surface scattering and Eq. (2) for grain boundary scattering, the combined analytical model for a rectangular metal wire is

$$\rho_{total} = \rho_{gr} + 0.46 \times (1-p) \times \left(\frac{\lambda_0}{w} + \frac{\lambda_0}{h}\right)\rho_0. \quad (4)$$

This model fits well with the measurement for metal wires of large sizes (>MFP). However, for metal wires of small sizes (≤MFP), the model is below the measurement; and the misfit increases as the metal wires' sizes decrease.

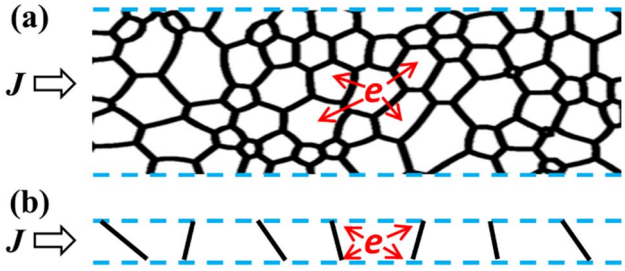

Fig. 1. Schematic cross-section of a metal wire or film composed of (a) multiple stacks of grains and (b) a single layer of grains.

III. Our Analytical Model

One possible reason for the misfit of the existing combined models in sub-MFP regime could be the inapplicability of Matthiessen's rule. While phonon scattering and grain boundary scattering are distributive and feasible for the use of Matthiessen's rule, surface scattering occurs only at the surfaces and should not be incorporated by simply applying the Matthiessen's rule.

We develop our analytical model by combining the FS model and MS model sequentially [9]. We start with an infinitely large bulk metal structure with resistivity-ρ_0 and MFP-λ_0. Adding grains in the bulk metal structure, the resistivity becomes $\rho_{\rm gr}$ after the MS model (Eq. (2)). The last step is to place surfaces to the existing metal structure and convert it into a metal wire or a metal film. The effect of the surfaces can be taken into account by applying the FS model. However, different from the grain-free metal structure studied in the original FS model, the metal wire or film under investigation has grains in it. Therefore, we have to replace the ρ_0 and λ_0 in the original FS model (Eq. (1)) with an effective resistivity-ρ^* and an effective MFP-λ^*, respectively. The ρ^* and λ^* are from the metal wire or film with grains but without considering the surface effect. Depending on how the grains distribute in the metal wire or film, we proceed with two cases: 1. metal wires or films that are composed of multiple stacks of grains (Fig. 1a); 2. metal wires or films that are composed of a single layer of grains (Fig. 1b). With grains in the metal wire or film, the resistivity depends on the direction of current flow. In both cases, the electrons flowing along the current directions would have to pass through series of grain boundaries. Thus, MS model is still valid, and $\rho^* = \rho_{\rm gr}$. However, λ^* accounts for the scatterings in all three dimensional directions (electrons are assumed to have equal chance in scattering towards any directions). For case 1 (Fig. 1a), electrons in the body of the metal structure would experience series of grain boundary scatterings before reaching the surfaces. Therefore, $\lambda^* = \lambda_{\rm gr}$, which follows [10]

$$\rho_{gr}\lambda_{gr} = \rho_0\lambda_0 = \frac{12\pi^3\hbar}{e^2 S_F}. \tag{5}$$

For case 2 (Fig. 1b), electrons in the body of the metal structure can reach the surfaces without passing through any grain boundaries (or only a few). Thus, λ^* is larger than $\lambda_{\rm gr}$, and would approach to λ_0 as the dimensions of the metal wire or film down-scale.

Replacing ρ_0 and λ_0 with $\rho_{\rm gr}$ and λ^* in the FS model (Eqn. (1)), the total resistivity of a rectangular metal wire becomes

$$\rho_{total} = \rho_{gr}\cdot\left[1 + 0.46\times(1-p)\times\left(\frac{\lambda^*}{w}+\frac{\lambda^*}{h}\right)\right]. \tag{6}$$

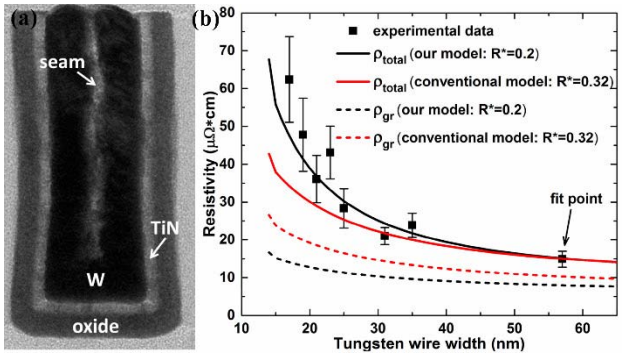

Fig. 2. (a) Cross-section TEM image of a representative TiN/W bi-layer wire. (b) Resistivity of W wires with constant height (~70 nm) and various widths.

For metal wires or films that are composed of multiple stacks of grains, $\lambda^* = \lambda_{\rm gr}$, and our model becomes the same as the conventional combined model as described in Eqn. (4). For metal wires or films that are composed of a single layer of grains, $\lambda^* \approx \lambda_0$, and our model becomes

$$\rho_{total} = \rho_{gr} + 0.46\times(1-p)\times\left(\frac{\lambda_0}{w}+\frac{\lambda_0}{h}\right)\rho_{gr}. \tag{7}$$

IV. Experiments and Results

W wires are widely used in advanced CMOS as interconnects. They are usually deposited via chemical vapor deposition (CVD) or physical vapor deposition (PVD). Because of W wires's small sizes, the W grains would expand to the half width of the wires [4]. Thus, W wires in CMOS fall into case 2 as shown in Fig. 1b.

Verification: TiN/W bi-layer wires of height (~70 nm) and widths from 24 to 64 nm were fabricated via the replacement gate process. A 2-3 nm TiN layer was first deposited as the diffusion barrier by atomic layer deposition (ALD). The W deposition was done by depositing a 2-nm ALD nucleation layer and then continuing with CVD W. Fig. 2a shows the cross-section TEM image of a representative TiN/W bi-layer wire. In this specific sample, we observed seams in the middle of the W wires. The seams were treated as the inner surfaces of the W wires in our modeling. It should be noted that there was air-break after the deposition of TiN (or WFM) and highly resistive native oxide would form after the air-break. Thus, we considered the total resistance of a TiN/W bi-layer wire to be the parallel resistance of the TiN layer and the W wire. Due to good conformality and uniformity of the ALD film, the resistance of the TiN layer is estimated from the measured resistivity of its thin film. We obtained the resistance and resistivity (symbols in Fig. 2b) of the W wires by removing the TiN resistance from the parallel resistance of the bi-layer wires.

Both our model (Eq. (7)) and the conventional model (Eq. (4)) were employed to model the W wires' resistivity. The ρ_0 and λ_0 of W are 5.3 $\mu\Omega\cdot$cm and 41 nm, respectively [11]. The p of W used here is 0 [12]. With the air-break induced native oxide sandwiched between TiN and W, the original p at W surfaces should be preserved at the W/TiN interfaces. Thus, we treated the W/TiN interfaces as W surfaces. The w and h of the W wires were extracted via TEM inspection. W grains in gate trenches would grow from the sidewalls to the middle (Fig. 2a). Therefore, the average

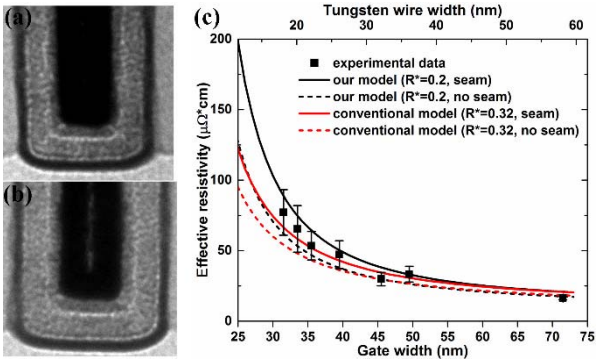

Fig. 3. (a) and (b) Tri-layer (WFM/TiN/W) metal gates without seam and with seam. (c) Measured and modeled effective resistivity of tri-layer metal gates with constant height (∼70 nm) and various widths.

grain size in the cross-section direction of a W wire is about half of the wire width [4]. Since the gate current is along the wires, D should be $1/2 \times w \times \beta$, where β is the factor between the average grain size along and across the W wires. Because the W deposition was done at high temperature and there was no post-deposition annealing, β should be ∼1. Without extracting an exact β, we simply assigned $D = 1/2 \times w$ and used an effective reflection co-efficient R*,

$$R^* = \frac{R}{\beta(1-R)+R}, \tag{8}$$

instead of the R in Eqn. (2) [13]. R denotes the average scattering strength of the potential at the grain boundaries. It depends not only on the intrinsic metal properties but also on the processing conditions because impurities segregated at the grain boundaries can increase the intrinsic R [14]. The W wires in our experiment are composed of ALD nucleation W and CVD W. The purity of the CVD W is very high, ∼99%. The ALD W nucleation layer may have a higher impurity level than the CVD W. However, since the ALD W constitutes only a small portion of any W wire in our experiment, the impact of the ALD W on the R of the W wires is expected to be small and could be negligible. For W wires with extremely small sizes, further investigation of the ALD W's impact may be needed. Within the small trench size range in our experiment, both β and R should be constant [14]. Therefore, R* should also be a constant. As the only unknown, we extracted R* by fitting the models to the experimental data at the largest width (with smallest uncertainty). The extracted R* is 0.2 for our model and 0.32 for the conventional model. The ρ_{total} and ρ_{gr} from both models using the extracted R* values are shown in Fig. 2b. As can be seen, our model fits better to the measurement in the whole width range than the conventional model especially for W wires with small widths. In another word, a constant R* can be found for our model, which verifies the correctness of our model.

Application: We also applied our model in modeling the resistance of tri-layer metal gates. The tri-layer metal gates are of height (∼70nm) and widths from 32 to 72 nm, and are composed of a 3-5 nm WFM layer, a 2-4 nm TiN and the W fill. The resistances of the TiN and WFM layers were calculated using their thin film resistivity via similar treatment as the bi-layer stack. The resistances of W wires were computed from both our model and the conventional model with the R* values extracted above. For this sample, we observed both seamed and seamless W wires (Fig. 3a and Fig. 3b). The seams were treated as surfaces and the seamless middle boundaries were treated as grain boundaries. Fig. 3c plots the measured and modeled effective resistivity of the metal gates. The upper and lower bounds of the experimental data are defined by our model simulated with and without seams, respectively. As can be seen, our model is in a good agreement with the measured data. For gate trenches that have negative-slope sidewalls, CVD W would pitch-off the trench openings and leave seams in the W wires. Thus, it is beneficial to have gate trenches that have straight or positive-slope sidewalls.

V. Conclusion

We propose an analytical metal resistance model for metal wires and films even with sub-MFP sizes. Our model includes surface, interface and grain boundary scatterings and proves to be useful in modeling and projecting the resistance of W metal gates in sub-22 nm CMOS.

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